AMENDMENT TO THE SPECIFICATION:

Amend the specification as follows:

Please replace the paragraph beginning at page 12, line 4, with the following rewritten paragraph:

Then the case is described in which a sinusoidal wave signal with a frequency higher than 1/2 D is received as the smoothing signal Shpp. As shown in Fig. 4, the smoothing signal Shpp shown in the section (a) is converted by the binarizing circuit 202 and the data converter 211 to the discrete value output signal Dpp shown in the section (b). The discrete value output signal Dpp is delayed and sign-negated by the delay/sign-negator 212 with the delay time D prolonged and the sign-negated, and is outputted as the delayed/sign-negated output signal Ddlpp as shown in the section (c). It is to be noted that, as a half cycle of the discrete value output signal Dpp is shorter than the delay time D in the delay/sign-negator 212, the delayed/sign-negated output signal Ddlpp has a rectangular waveform with a phase different from that of the discrete value output signal Dpp. Therefore, when the delayed/sign-negated output signal Ddlpp and the delayed/sign-negated output signal ~~Ddlpp~~ Dpp are multiplied by the multiplier 213, the multiplied value output signal Dprd generated as described above and as shown in the section (d) take positive or negative discrete values at the probability of about 50% respectively. Therefore, when the multiplied value output signal

Dprd is integrated by the integrator 214, the multiplied value output Dint does not amplify almost at all as shown in the section (e). Thus, when a sinusoidal wave signal with a frequency higher than 1/2 D is received as the smoothing signal Shpp, the autocorrelation computing circuit 210 does not amplify the integrated value output signal almost at all.